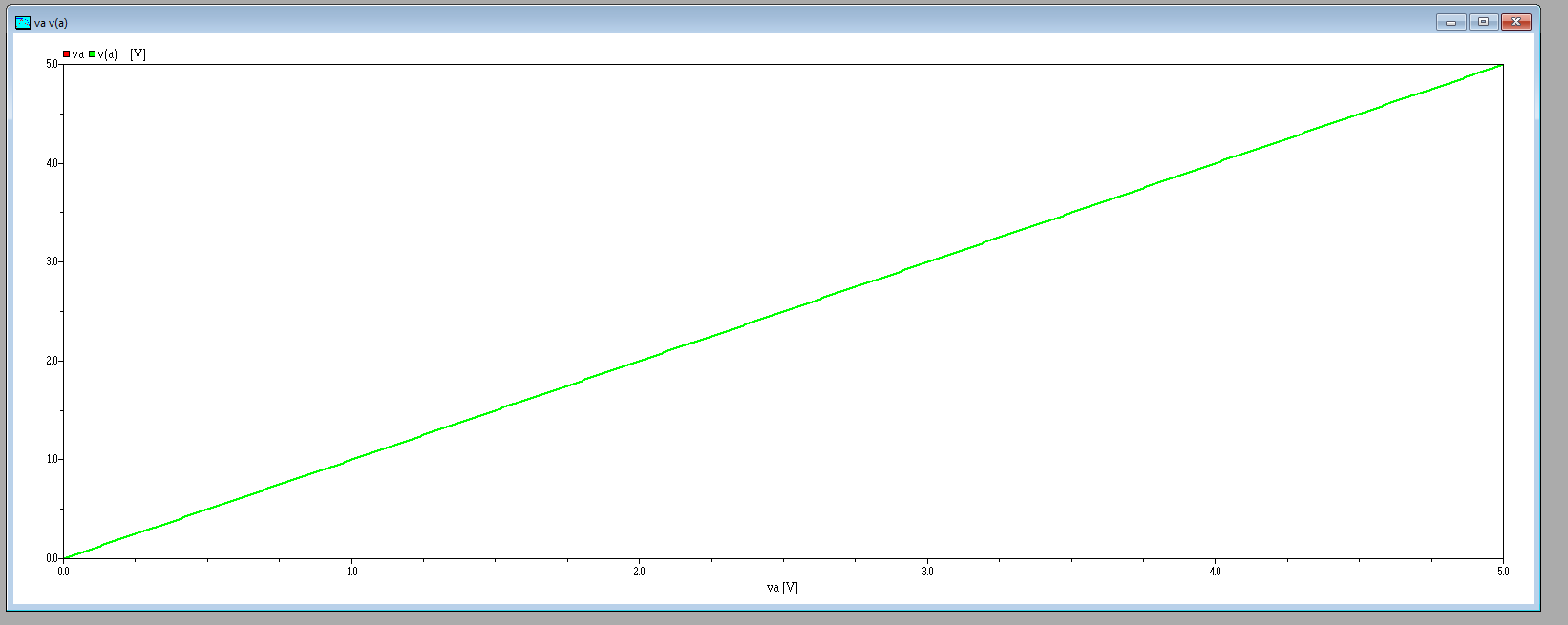
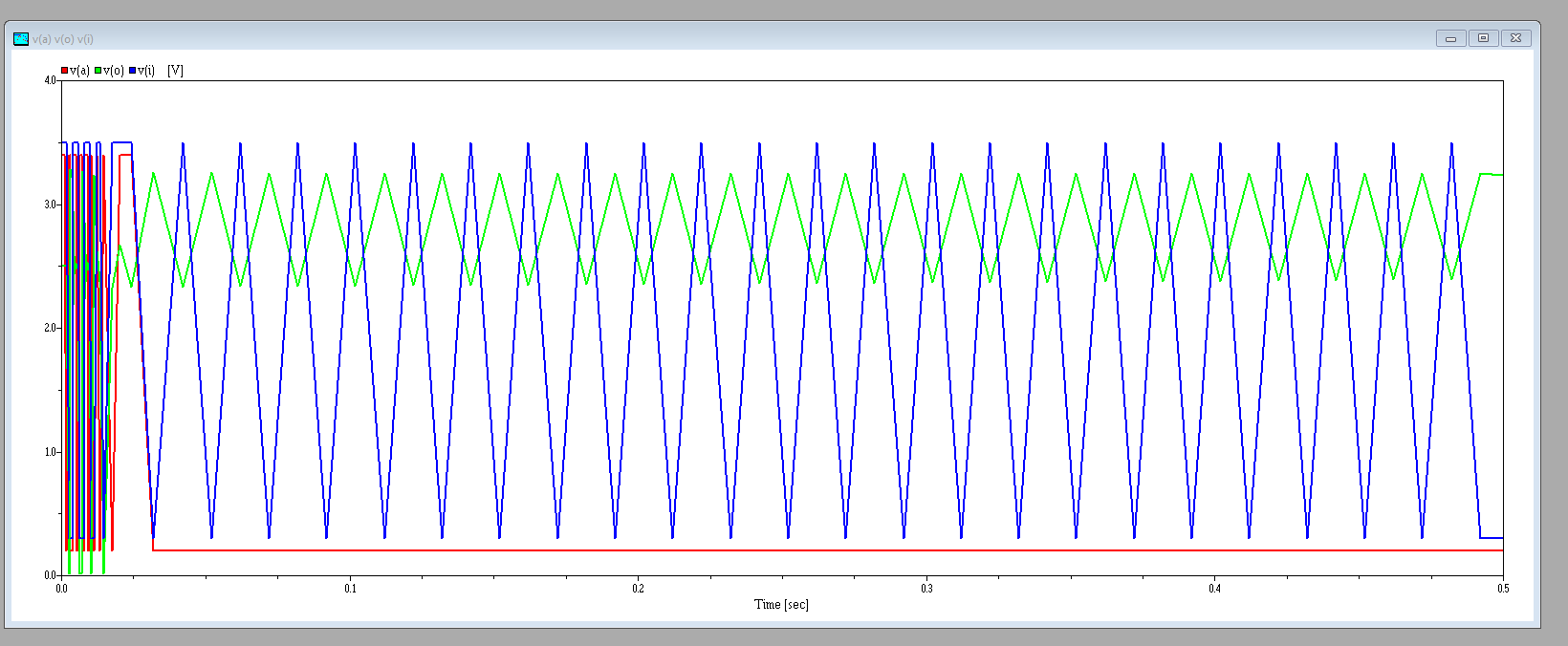
In this lab we used tri-state to design busses.

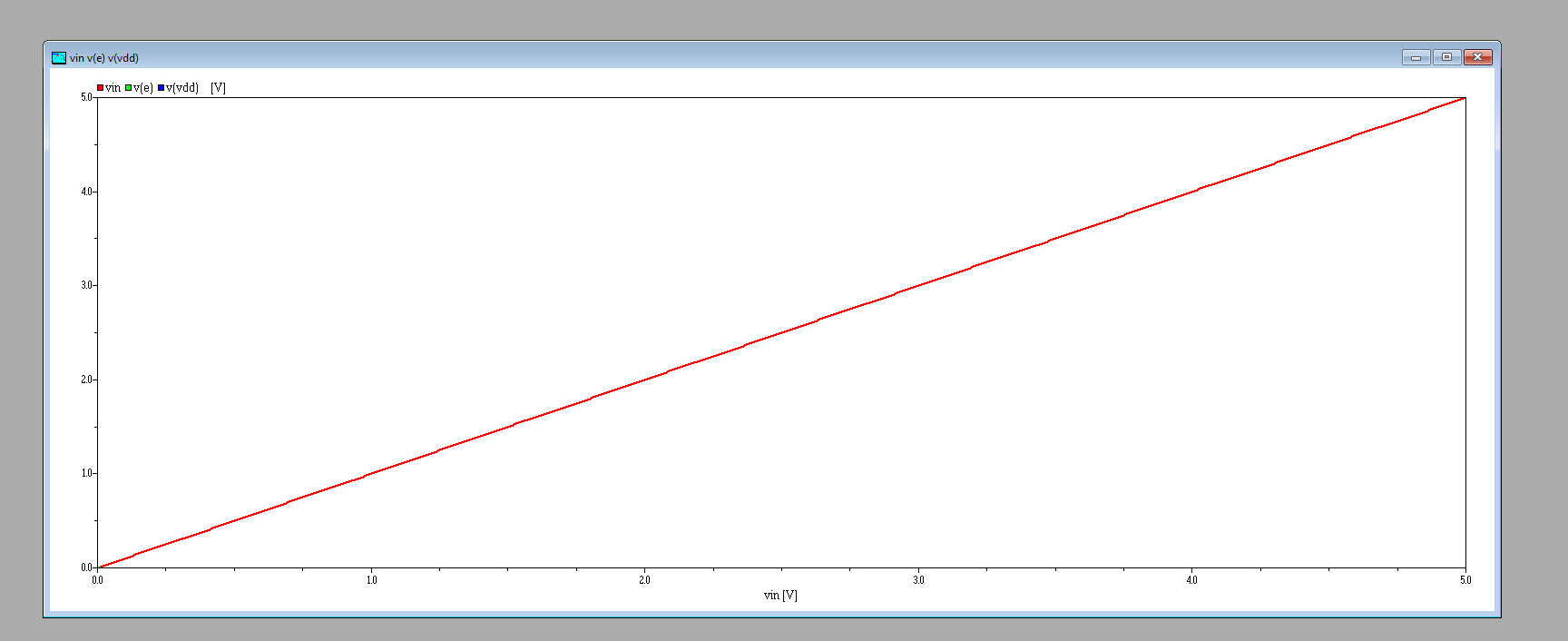
TTL DC Analysis:



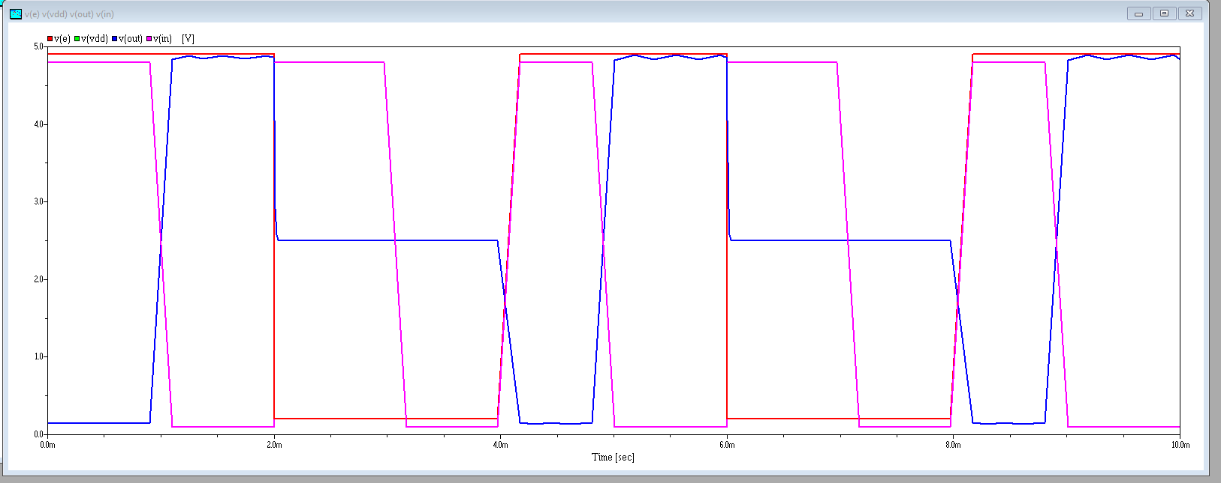
TTL TR Analysis :



CMOS DC :



CMOS Voltage Diver equal Values :



CMOS Voltage Divide, R1 modified to 1e5

